

180831368 Si838x Product Revision For The Low Pass Debounce Filter Operation

PRCN Issue Date: 8/31/2018

Effective Date: 12/6/2018

PCN Type: Product Revision

Description of Change

Silicon Labs is announcing a new revision to the Si838x product family. The revision corrects an issue with the low pass debounce filter(available on a subset of products) where periodic input signals may cause the filter to malfunction. The new revision behaves as defined in the current data sheet.

The new revision is indicated on the Si838x package by the number 1823 or higher in the first four digits of the line 2 marking. Consult section 9 of the Si838x datasheet for top marking details.

Reason for Change

To correct operation of the low pass debounce filter on select Si838x OPNs to match the data sheet description.

Impact on Form, Fit, Function, Quality, Reliability

The debounce filter function has changed to match the published data sheet. No other changes to functionality were made.

Product Identification

Si8380S-IU Si8380S-IUR Si8380PS-IU Si8380PS-IUR Si8380PM-IU Si8380PM-IUR Si8380PF-IU Si8380PF-IUR Si8382PS-IU Si8382PS-IUR Si8382PM-IU Si8382PM-IUR Si8382PF-IU Si8382PF-IUR Si8384PS-IU Si8384PS-IUR Si8384PM-IU Si8384PM-IUR Si8384PF-IU Si8384PF-IUR

Last Date of Unchanged Product: 12/6/2018

Qualification Samples

Available Upon Request.

Customer Response

Lack of acknowledgment of the PCN within 30 days constitutes acceptance of the change, Ref. JEDEC-J-STD-046.

To request further data or inquire about this notification, please contact your Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at http://www.silabs.com.

Customers may approve early PCN acceptance by emailing approval, along with PCN # to PCNEarlyAcceptance@silabs.com

User Registration

Register today to create your account on Silabs.com. Your personalized profile allows you to receive technical document updates, new product announcements, "how-to" and design documents, product change notices (PCN) and other valuable content available only to registered users. <u>http://www.silabs.com/profile</u>

Qualification Data

Please see the below Qualification Report.

Si838x 20-Pin QSOP AEC-Q100 Qualification Report

W7101F1 - Product Qualification Report Record Rev. H

SILICON LABS The information contained in this document is PROPRIETARY to Silicon Laboratories, Inc. and shall not be reproduced or used in part or whole without Silicon Laboratories' written consent. The document is uncontrolled if printed or electronically saved.

Part Rev A, Vanguard Fabrication, UTACTH Assembly except as noted							
-				Fail/Pass or			
Test Name	Test Condition	Qualification	Start	End	Notes	Summary	Status
Test Group A – Ad HAST	ccelerated Environment Stres	s Tests					
	JA110		Q038511	0/85	1, 2		_
	130°C, 85%RH	3 lots, N=>77	Q039657	0/85	1, 2	3 lots	Pass
	Vcc=5.5V, 96 hours		Q039656	0/85	1, 2	0/255	
UHAST	JA110		Q038513	0/85	1, 2		
	130°C, 85%RH	3 lots, N=>77	Q039659	0/85	1, 2	3 lots	Pass
	Vcc=5.5V, 96 hours		Q039658	0/85	1, 2	0/255	
Temp Cycle	JA104		Q038407	0/85	1, 2		
	Cond C: -65°C to 150°C	3 lots, N=>77	Q039660	0/85	1, 2	3 lots	Pass
	500 cycles		Q039661	0/85	1, 2	0/255	
HTSL	JA103						
	150°C, 1000hr	1 lot, N=>45	Q038154	0/50	1, 2	1 lots	Pass
						0/50	
Test Group B – Ad	ccelerated Lifetime Simulation	n Tests					
HTOL	JA108		Q038519	0/100	3		
	T _J ≥ 125°C, Dynamic	3 lots, N=>77	Q039664	0/81	3	3 lots	Pass
	Vcc=5.5V, 1000 hours		Q039665	0/100	3	0/281	
ELFR	AEC-Q100-008		Q038177	0/822	3		
	T _J ≥ 125°C, Dynamic	3 lots, N=>800	Q039663	0/819	3	3 lots	Pass
	Vcc=5.5V, 48 hours		Q043137	0/818		0/2459	
Test Group C – Pa	ackage Assembly Integrily Te	sts					
Wire Bond Shear	AEC-Q100-001		718170	0/6			
		5 units, N=>30	721740	0/6		3 lots	Pass
			721741	0/6		0/18	
Wire Bond Pull	M-STD-883		718170	0/6			
	Performed post-TC	5 units, N=>30	721740	0/6		3 lots	Pass
	i chomico postero		721741	0/6		0/18	1 400
Physical Dimensior	INS UR100		718170	0/30		VIIU	
	00100	3 lots, N=>10	721740	0/30		3 lots	Pass
		0.000, 11-2.10	721740	0/30		0/90	1 0 0 0
Solderability	JB102		718170	0/10		0100	
	00102	1 lot, N=>15	721740	0/10		3 lata	Pass
		1100, 14=215				3 lots	Pass
			721741	0/10		0/30	

Si838x 20-Pin QSOP AEC-Q100 Qualification Report

W7101F1 - Product Qualification Report Record Rev. H

SILICON LABS The information contained in this document is PROPRIETARY to Silicon Laboratories, Inc. and shall not be reproduced or used in part or whole without Silicon Laboratories' written consent. The document is uncontrolled if printed or electronically saved.

Part Rev A, Va	Part Rev A, Vanguard Fabrication, UTACTH Assembly except as noted						
			Lot ID or Fail/Pass or				
Test Name	Test Condition	Qualification	Start	End	Notes	Summary	Status
Test Group E – E	lectrical Verification						
ESD-HBM	AEC-Q100-002	1 lot, N=>3	Q043138				Class 3A
ESD-CDM	AEC-Q100-011	1 lot, N=>3	Q043139				Class C5
Latch Up	AEC-Q100-004 ±200mA Overvoltage = 8.25V	1 lot, N=>6	Q043140	125 °C			Pass

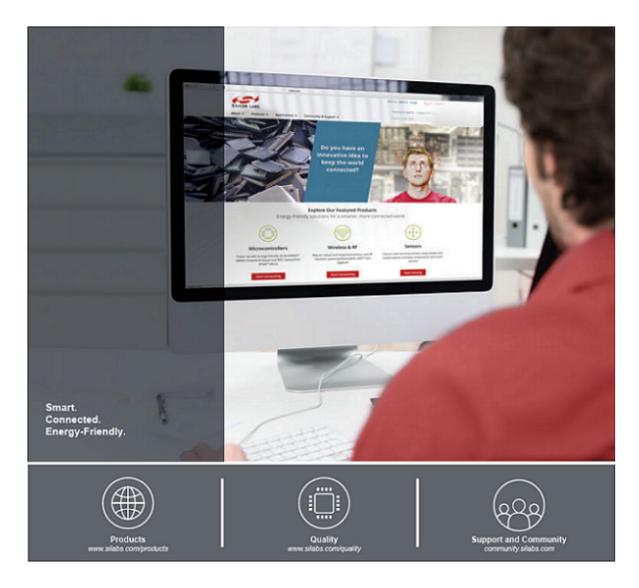
Notes:

1. Parts are Pre-conditioned at MSL2/260°C

2. Leveraged package family qualification data

3. Leveraged die family qualification data

This report applies to the following part numbers:					
SI8380P-IU/R	SI8380PF-IU/R	SI8380PM-IU/R	SI8380PS-IU/R	SI8380S-IU/R	
SI8382P-IU/R	SI8382PF-IU/R	SI8382PM-IU/R	SI8382PS-IU/R	SI8384P-IU/R	
SI8384PF-IU/R	SI8384PM-IU/R	SI8384PS-IU/R	SI8388P-IU/R		



Disclaimer

Silicon Labs intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Labs products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Labs reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Labs shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any Life Support System without the specific written consent of Silicon Labs. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if fails, can be reasonably expected to result in significant personal injury or death. Silicon Labs products are not designed or authorized to key set on the ass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

Trademark Information

Silicon Laboratories Inc.®, Silicon Laboratories®, Silicon Labs®, SiLabs® and the Silicon Labs logo®, Bluegiga®, Bluegiga Logo®, Clockbuilder®, CMEMS®, DSPLL®, EFM®, EFM32®, EFR, Ember®, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZRadio®, EZRadioPRO®, Gecko®, ISOmodem®, Micrium, Precision32®, ProSLIC®, Simplicity Studio®, SiPHY®, Telegesis, the Telegesis Logo®, USBXpress®, Zentri and others are trademarks or registered trademarks of Silicon Labs. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc. 400 West Cesar Chavez Austin, TX 78701

http://www.silabs.com